WHAT IS CLAIMED IS:

1. A method of providing data processor emulation information, comprising:

providing a program counter trace stream of program counter values used by a data processor;

inserting a synchronization marker into the program counter trace stream; and

providing trace information indicative of a data processing operation performed by the data processor, including identifying a program counter value that corresponds to the data processing operation, said identifying step including expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

2. The method of Claim 1, wherein said data processing operation is a memory access operation.

3. The method of Claim 1, wherein said identifying step includes detecting occurrences of program counter loads in the data processor.

4. The method of Claim 3, wherein said identifying step includes counting detected occurrences of program counter loads.

5. The method of Claim 4, wherein said identifying step includes maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker.

6. The method of Claim 5, including inserting a further synchronization marker into the program counter trace stream, and setting said running count to a predetermined value in response to insertion of said further synchronization marker.

7. The method of Claim 5, wherein said maintaining step includes updating said running count in response to an occurrence of a program counter load associated with said corresponding program counter value, said identifying step including defining said offset to be equal to said running count as updated by said updating step.

8. The method of Claim 7, including inserting a further synchronization marker into the program counter trace stream, and setting said running count to a predetermined value in response to insertion of said further synchronization marker.

9. The method of Claim 7, wherein said trace information providing step includes providing a further trace stream that includes said trace information, and further including inserting the offset in said further trace stream.

10. The method of Claim 1, wherein said trace information providing step includes providing a further trace stream that includes said trace information, and further including inserting the offset in said further trace stream.

11. The method of Claim 10, including combining the program counter trace stream and said further trace stream into a composite stream.

12. The method of Claim 1, wherein said identifying step includes expressing said corresponding program counter value as a native program counter value unless a program counter trace condition exists.

13. An apparatus for providing data processor emulation information, comprising:

first and second inputs for coupling to a data processor;

a trace stream generator coupled to said first input for providing a program counter trace stream of program counter values used by the data processor, said trace stream generator operable for inserting a synchronization marker into the program counter trace stream; and

a trace apparatus coupled to said second input for providing trace information indicative of a data processing operation performed by the data processor, including a program counter identifier for identifying a program counter value that corresponds to said data processing operation, said program counter identifier operable for expressing

said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

14. The apparatus of Claim 13, wherein said program counter identifier is responsive to information received from the data processor for detecting occurrences of program counter loads in the data processor.

15. The apparatus of Claim 14, wherein said program counter identifier includes a counter for counting detected occurrences of program counter loads.

16. The apparatus of Claim 15, wherein said counter is operable for maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker.

17. The apparatus of Claim 16, wherein said counter is operable for setting said running count to a predetermined value in response to insertion of the synchronization marker.

18. The apparatus of Claim 13, wherein said trace apparatus includes a further trace stream generator for providing a further trace stream that includes said trace information and said offset.

19. The apparatus of Claim 18, including a combiner coupled to said trace stream generators and operable for combining said program counter trace stream and said further trace stream into a composite trace stream.

20. The apparatus of Claim 13, wherein said data processing operation is a memory access operation.

21. The apparatus of Claim 13, wherein said program counter identifier includes an input for receiving information indicative of insertion of the synchronization marker.

22. The apparatus of Claim 21, wherein said program counter identifier input is coupled to said trace stream generator.

23. An integrated circuit, comprising:

a data processor for performing a data processing operation; and

an apparatus coupled to said data processor for providing emulation information about said data processing operation, including a trace stream generator for providing a

program counter trace stream of program counter values used by said data processor, said trace stream generator operable for inserting a synchronization marker into the program counter trace stream, and a trace apparatus for providing trace information indicative of said data processing operation, said trace apparatus including a program counter identifier for identifying a program counter value that corresponds to said data processing operation, said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

24. A data processing system, comprising:

an integrated circuit, including a data processor for performing a data processing operation;

an emulation controller coupled to said integrated circuit for controlling emulation operations of said data processor; and

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for providing emulation information about said data processing operation, said apparatus including a trace stream generator for providing a program counter trace stream of program counter values used by said data processor, said trace stream generator operable for inserting a synchronization marker into the program counter trace stream, and said apparatus further including a trace apparatus for providing trace information indicative of said data processing operation, said trace apparatus

including a program counter identifier for identifying a program counter value that corresponds to said data processing operation, said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

25. The system of Claim 24, including a man/machine interface coupled to said emulation controller for permitting a user to communicate with said emulation controller.

26. The system of Claim 25, wherein said man/machine interface includes one of a visual interface and a tactile interface.